Amendments to the Claims:

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of Claims:

1. (currently amended) A circuit component comprising:

a semiconductor substrate;

a metallization structure over said semiconductor substrate;

a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a top surface of said metallization structure; and

a patterned circuit layer connected to said top surface through said opening, wherein said patterned circuit layer comprises a first portion used to have a bump formed thereover, [[and]] a second portion comprising a gold layer and a third portion used to be wirebonded thereto, wherein said gold layer is used to be in contact with a testing probe, and wherein said first portion is connected to said second portion.

2. (canceled)

3. (previously presented) The circuit component of Claim 1, wherein said gold layer has a thickness of greater than 1 micron.

4. (canceled)

5. (previously presented) The circuit component of Claim 1, wherein said patterned circuit layer comprises a nickel layer under said gold layer.

6. (previously presented) The circuit component of Claim 1, wherein said patterned circuit layer comprises a copper layer under said gold layer.

7. (previously presented) The circuit component of Claim 1, wherein said patterned circuit layer further comprises a copper layer and a nickel layer over said copper layer, and wherein said gold layer is over said nickel layer.

8. (previously presented) The circuit component of Claim 1 further comprising a polymer layer between said passivation layer and said patterned circuit layer.

9. (previously presented) The circuit component of Claim 8, wherein said polymer layer comprises polyimide.

10. (previously presented) The circuit component of Claim 1 further comprising a polymer layer on said patterned circuit layer, multiple openings in said polymer layer exposing said first and second portions.

11. (previously presented) The circuit component of Claim 10, wherein said polymer layer comprises polyimide.

Claim 12 (canceled)

13. (previously presented) The circuit component of Claim 1, wherein said patterned circuit layer comprising a metal line connecting said first and second portions.

Claim 14 (canceled)

15. (previously presented) The circuit component of Claim 1, wherein said passivation

layer comprises a topmost nitride layer of said circuit component.

16. (previously presented) The circuit component of Claim 1, wherein said passivation layer has a thickness of greater than 0.35 μm.

17. (currently amended) The circuit component of Claim 1 further comprising a bump over ~~on~~ said first portion.

18. (previously presented) The circuit component of Claim 17 further comprising a nickel layer between said bump and said first portion.

19. (previously presented) The circuit component of Claim 17, wherein said bump comprises solder.

20. (previously presented) The circuit component of Claim 17 further comprising a copper layer between said bump and said first portion.

21. (previously presented) The circuit component of Claim 17, wherein said bump comprises a lead-free alloy.

Claims 22 and 23 (canceled)

24. (currently amended) The circuit component of Claim 1[[23]], wherein said patterned circuit layer comprises a metal trace connecting said second and third portions.

25. (previously presented) The circuit component of Claim 1, wherein a pitch between said first and second portions is less than 300 μm.

26. (previously presented) The circuit component of Claim 1, wherein a pitch between said first and second portions is less than 1 millimeter.

27. (previously presented) A circuit component comprising:

a semiconductor substrate;

a metallization structure over said semiconductor substrate;

a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a top surface of said metallization structure; and

a patterned circuit layer connected to said top surface through said opening, wherein said patterned circuit layer comprises a first portion used to have a bump formed thereover and a second portion comprising a copper layer, wherein said copper layer is used to be wirebonded thereover.

28. (previously presented) The circuit component of Claim 27, wherein said patterned circuit layer further comprises a titanium-containing layer under said copper layer.

29. (previously presented) The circuit component of Claim 27, wherein said patterned circuit layer further comprises a chromium-containing layer under said copper layer.

30. (previously presented) The circuit component of Claim 27 further comprising a polymer layer between said passivation layer and said patterned circuit layer.

31. (previously presented) The circuit component of Claim 30, wherein said polymer layer comprises polyimide.

32. (previously presented) The circuit component of Claim 27 comprising a polymer layer on said patterned circuit layer, multiple openings in said polymer layer exposing said first and second portions.

33. (previously presented) The circuit component of Claim 32, wherein said polymer layer comprises polyimide.

34. (previously presented) The circuit component of Claim 27, wherein said patterned circuit layer comprises a metal line connecting said first and second portions.

35. (previously presented) The circuit component of Claim 27, wherein said patterned circuit layer comprises a third portion used to be in contact with a testing probe.

Claim 36 (canceled)

37. (previously presented) The circuit component of Claim 35, wherein said patterned circuit layer comprises a metal trace connecting said first and third portions.

38. (previously presented) The circuit component of Claim 27, wherein said passivation layer has a thickness of greater than 0.35 μm.

39. (previously presented) The circuit component of Claim 27, wherein said passivation layer comprises a topmost nitride layer of said circuit component.

40. (previously presented) The circuit component of Claim 27 further comprising a bump over said first portion.

41. (previously presented) The circuit component of Claim 40, wherein said bump comprises solder.

42. (previously presented) The circuit component of Claim 40 further comprising a nickel

layer between said bump and said first portion.

43. (previously presented) The circuit component of Claim 40, wherein said bump comprises a lead-free alloy.

44. (previously presented) The circuit component of Claim 27 further comprising a wirebonded wire bonded over said second portion.

Claim 45 (canceled)

46. (previously presented) A circuit component comprising:

a semiconductor substrate;

a metallization structure over said semiconductor substrate;

a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a top surface of said metallization structure; and

a patterned circuit layer connected to said top surface through said opening, wherein said patterned circuit layer comprises a first portion used to be wirebonded thereto and a second portion used to be in contact with a testing probe.

47. (previously presented) The circuit component of Claim 46, wherein said patterned circuit layer comprises gold.

48. (previously presented) The circuit component of Claim 46, wherein said patterned circuit layer comprises a gold layer having a thickness of greater than 1 micron.

49. (previously presented) The circuit component of Claim 46, wherein said patterned circuit layer comprises copper.

50. (previously presented) The circuit component of Claim 46, wherein said patterned circuit layer comprises nickel.

51. (previously presented) The circuit component of Claim 27, wherein said second portion further comprises a nickel layer over said copper layer, and wherein said nickel layer is used to be said wirebonded thereover.

52. (previously presented) The circuit component of Claim 27, wherein said second portion further comprises a gold layer over said copper layer, and wherein said gold layer is used to be said wirebonded thereon.